REMARKS

In the Office Action mailed May 23, 2002:

The abstract of the disclosure was objected to because it was missing from the application.

The disclosure was objected to because "Fig. 6" should have been referred to as "Figs. 6A-D at page 22, line 26 and no description was provided for Figs. 17A-B at page 23, line 24.

Claims 85-87 and 100 were rejected under 35 U.S.C. 102(b) as anticipated by Jacobsen (U.S. Patent 5,673,131) and as anticipated by Zappe (U.S. Patent 3,983,546).

In response, an abstract has been supplied, the description of Figs. 6A-D has been corrected and the brief description of Figs. 17A-B has been supplied. No new matter has been added.

Applicant's claimed invention relates to an apparatus for communicating or signalling between integrated circuit (IC) chips, modules or substrates using capacitive coupling rather than conductive paths. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect signalling between different chips and modules, the prior art requires the use of conductive connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling capacitively. As described beginning at page 25, line 16, pairs of half-capacitor plates (Fig. 1, elements 15, 14), one half located on each IC chip (11), module or substrate (10), are used to capacitively couple signals from one IC chip, module or substrate to another. The use of such plates relaxes the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

Jacobsen discloses a three-dimensional circuit structure. The preferred structures appear to be cylindrical structures such as fiber optic strands. Circuits are described as being formed on the surface of such structures using non-planar exposure beam lithography. In conjunction with Fig. 9B of the '131 patent, Jacobsen describes capacitive coupling between

capacitor plates such as elements 214 and 216 on cylindrical substrates 212, 210, respectively.

Zappe discloses Josephson tunneling devices that are used as parametrons. With reference to Fig. 14, Zappe states at col. 12, lines 58-67:

> In operation, conductive plates 170A and 170B are capacitively coupled and transmit information there-between at a frequency F_1. In the same manner, information is transmitted between conductive plates 172A and 172B at a frequency F_2. At the frequencies used for Josephson circuitry (10^{11} - 10^{12} Hz) capacitive coupling between conductive plates located on separate circuit chips is sufficient to provide communication between the chips without the requirement for interconnecting wires.

It is to be noted that Josephson Junction circuits are superconducting circuits, not semiconducting circuits.

Independent claims 86 and 100 recite a method of capacitively coupling signals between first and second chips. At page 183, *The New IEEE Standard Dictionary of Electrical and Electronic Terms* (IEEE, 5th Ed., January 15, 1993) defines a chip as "A small unpackaged functional element made by subdividing a wafer of semiconductor material. Sometimes referred to as a 'die.'" A copy of page 183 is enclosed.

In view of the foregoing definition, it would appear that the word "chip" is well understood in the industry to refer to a semiconductor. Nevertheless, to make clear that the chip referred to is a semiconductor, claims 86 and 100 have been amended to recite a "semiconductor chip."

With respect to Jacobsen, the Examiner has taken the position that the cylindrical substrates of Jacobsen are cylindrically shaped chips and has rejected the claims as anticipated by Jacobsen under 35 U.S.C. 102(e). Applicants must respectfully disagree. It is apparent that the substrates of Fig. 9B of Jacobsen are cylinders such as optical fibers and not chips. The substrates are three-dimensional objects that plainly were not formed from a wafer and plainly were not made by subdividing a wafer. The differences between the structure and operation of the three-dimensional devices of Jacobsen and conventional planar devices

constitute the point of novelty between Jacobsen and the prior art as set forth in his patents and his file wrappers.

Accordingly, claims 86 and 100 define over Jacobsen in reciting capacitive coupling of signals between semiconductor chips. Nor does Jacobsen suggest capacitive coupling of chips. Jacobsen's cylinders are three-dimensional objects with shapes very different from those of chips. Whatever might work with Jacobsen's cylinders does not suggest what will work in the case of a chip on a substrate. For these reasons, claims 86 and 100 are believed to be patentable over Jacobsen.

Claims 86 and 100 are also believed to define over Zappe because Zappe does not disclose a semiconductor device. Rather, his Josephson devices are superconductors. Superconductors are very different from semiconductors. Zappe is interested in new applications for Josephson tunneling devices and, in particular, in the use of such devices at very high frequency parametrons. In addition, he is interested in the use of Josephson tunneling devices or circuit interconnection. He states at Col. 1, lines 35-37 that:

> "The prior art has also not addressed the problem of interconnections between circuit chips having circuits thereon for memory and logic functions. Such functions could be performed by Josephson tunneling devices or by other electrical components."

But Zappe does not in fact solve this prior art problem. There are no Josephson tunneling devices that work as memories, i.e., that latch (hold) a binary value. And, all logic devices formed with Josephson devices are likewise limited to the non-latching variety.

Furthermore, by the phrase "other electrical components," Zappe turns out to mean solely alternatives which are themselves Josephson tunneling electrical components. Zappe offers no further disclosure whatsoever regarding circuit chips other than those containing superconducting Josephson tunneling devices and operating at cryogenic temperatures. Zappe never teaches or describes any logic, memory, or other electrical components which are non superconducting, much less semiconducting. He is simply silent on the subject of non-superconducting components.

Zappe's failure to deal with non-superconducting electronics is important because the circuit topologies and logic gates needed to enable a superconducting version are in every case incompatible with the non-superconducting versions. Teaching an apparatus for superconducting does not teach the non-superconducting circuit. Enabling an apparatus for superconducting does not enable the non-superconducting circuit. The two technologies are not analogous. Nothing in Zappe's patent would have changed if semiconductors had never come along.

Specifically, the Josephson tunneling devices he describes are Josephson oscillators, which have no non-superconducting equivalent; and parametrons, which measure minute changes in magnetic flux density. Since magnetic flux density is approximately one millionth as energetic as electric current, the semiconductor analog of a parametron is neither practical or feasible. Superconducting Josephson tunneling junctions can nevertheless detect such small magnetic changes. However, superconducting circuits cannot latch (retain) a logic state; also, superconducting circuits do not impart gain. As a result, superconducting circuits are vastly different from the latching, semiconductor configurations claimed in claim 100 and disclosures in one technology do not suggest the other.

Dependent claim 87 is believed patentable for the same reason 86 is patentable.

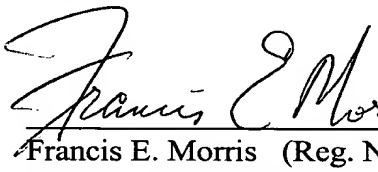
Independent claim 85 recites a method of sending data from a first module to a second module using first and second half-capacitors in a modular digital system. Jacobsen and Zappe do not disclose or suggest such a modular digital system. Fig. 9b of Jacobsen discloses a three-dimensional bundle of spaced-apart elongated cylindrical structures. Zappe merely discloses a variety of superconducting Josephson circuits. The term module, however, is defined at page 3, lines 8-11 of the application to refer to "one or more Level 0 dies, one or more Level 1 or Level 0 chips (packaged or not) and of course higher order ensembles." The elongated cylinders of Jacobsen are simply not the dies or chips or higher order ensembles of applicants' claim 85 and they make no suggestion of such modules because these cylinders are such unusual structures. Likewise, the superconducting circuits of Zappe are not the semiconductor dies or chips or higher order ensembles of applicants' claim 85 and they make no suggestion of such modules because Zappe's superconducting circuits are not semiconductors.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully requests the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (650) 849-7777 so that any remaining issues may be resolved.

Aside for the Petition for Extension of Time fee, no additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date November 22, 2002



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APPENDIX A

Changes to the Specification

The paragraph at page 22, line 26 is revised as follows:

Fig. 6A-D depict the exemplary waveforms for a digital (or multistate) signal capacitively coupled from a die to a substrate in accordance with the invention;

Insert at page 23, before line 25:

--Figs. 17A-B depict connection methods in accordance with the prior art and the present invention;--

APPENDIX B

Changes to the Claims

The rewritten claims were revised as follows:

86. (Amended) A method of coupling signals between electronic devices in a modular electronic system, said method comprising the steps of:

locating a first subset of said electronic devices on a first semiconductor chip;

locating a second subset of said electronic devices on a second semiconductor chip; and,

aligning and affixing said first and second chips so as to capacitively couple said first and second chips.

100. (Amended) A method of capacitively coupling signals between first and second semiconductor chips, each said chip having a plurality of half-capacitors, said method comprising the steps of:

affixing said first chip to a substrate;

aligning said second chip to said first chip; and,

affixing said second chip to said substrate, thereby capacitively coupling corresponding half-capacitors on said first and second chips and providing direct capacitive coupling between said first and second chips.

APPENDIX C

ABSTRACT

The Abstract was not filed with application. Please insert the following Abstract.

--Methods and apparatus are described for capacitively signaling between different semiconductor chips and modules without the use of connectors, solder bumps, wire-bond interconnections or the like. Preferably, pairs of half-capacitor plates, one half located on each chip, module or substrate are used to capacitively couple signals from one chip, module or substrate to another. The use of plates relaxes the need for high precision alignment as well as reduces the area needed to effect signaling, and reduces or eliminates the requirements for exotic metallurgy.--

IEEE Std 100-1992

The New IEEE Standard Dictionary of Electrical and Electronics Terms

[Including Abstracts of All Current IEEE Standards]

Fifth Edition

Gediminas P. Kurpis, Chair

Christopher J. Booth, Editor

IEEE

check, transfer (electronic computation). *See:* **transfer check.**

check valve. *See:* **blocking capacitor.**

cheek, field-coil flange (washer). *See:* **collar.**

cheese antenna. A reflector antenna having a cylindrical reflector enclosed by two parallel conducting plates perpendicular to the cylinder, spaced more than one wavelength apart. *Syn:* **pillbox antenna.** 145-1983

chemical conversion coating. A protective or decorative coating produced in situ by chemical reaction of a metal with a chosen environment. [59]

chemical vapor deposition (CVD) technique (fiber optics). A process in which deposits are produced by heterogeneous gas-solid and gas-liquid chemical reactions at the surface of a substrate. *Note:* The CVD method is often used in fabricating optical waveguide preforms by causing gaseous materials to react and deposit glass oxides. Typical starting chemicals include volatile compounds of silicon, germanium, phosphorus, and boron, which form corresponding oxides after heating with oxygen or other gases. Depending upon its type, the preform may be processed further in preparation for pulling into an optical fiber. *See:* **preform.** 812-1984

Chicago grip. *See:* **conductor grip.** 516-1987

chief programmer (software). The leader of a chief programmer team; a senior-level programmer whose responsibilities include producing key portions of the software assigned to the team, coordinating the activities of the team, reviewing the work of the other team members, and having an overall technical understanding of the software being developed. *See also:* **backup programmer; chief programmer team.** 610.12-1990

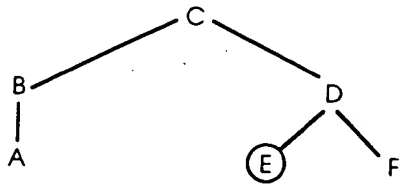
chief programmer team (software). A software development group that consists of a chief programmer, a backup programmer, a secretary/librarian, and additional programmers and specialists as needed, and that employs procedures designed to enhance group communication and to make optimum use of each member's skills. *See also:* **backup programmer; chief programmer; egoless programming.** 610.12-1990

Child-Langmuir equation (thermionics). An equation representing the cathode current of a thermionic diode in a space-charge-limited-current state.

$I = GV^{3/2}$

where I is the cathode current, V is the anode voltage of a diode or the equivalent diode of a triode or of a multi-electrode value or tube, and G is a constant (perveance) depending on the geometry of the diode or equivalent diode. *See:* **electron emission.** [45], [84]

child node. In a tree, a descendant node having a given node as its parent node. *Syn:* **daughter; son.** *Contrast with:* **parent node.** *See also:* **sibling node.** 610.5-1990



E is a Child Node of Node D

child segment. In a hierarchical database, a segment that has a parent segment and that is dependent on that segment for its existence. *Note:* If the parent segment is deleted, the child segment must be deleted. *Contrast with:* **parent segment.** *See also:* **dependent segment; logical child segment; physical child segment; twin segment.** 610.5-1990

Chinese binary. *See:* **column binary.** 610.1

chip (1) (mechanical recording). The material removed from the recording medium by the recording stylus while cutting the groove. *See:* **phonograph pickup.** [32]
(2) (semiconductor) (nonlinear, active, and nonreciprocal waveguide components). A small unpackaged functional element made by subdividing a wafer of semiconductor material. Sometimes referred to as a "die." 457-1982

chip enable (E) (semiconductor memory). The inputs that when true permit input, internal transfer, manipulation, refreshing, and output of data, and when false cause the memory to be in a reduced power standby mode. *Note:* Chip enable is a clock or strobe that significantly affects the power dissipation of the memory. Chip select is a logical function that gates the inputs and outputs. For example, chip enable may be the cycle control of a dynamic memory or a power reduction input on a static memory. 662-1980w

chip-on-board testing. A test of a component after it has been assembled onto a printed circuit board or other substrate; for example, using the facilities defined by IEEE Std 1149.1-1990. 1149.1-1990

chip select (S) (semiconductor memory). The inputs that when false prohibit writing into the memory and disable the output of the memory. *Note:* Chip enable is a clock or strobe that significantly affects the power dissipation of the memory. Chip select is a logical function that gates the inputs and outputs. For example, chip enable may be the cycle control of a dynamic memory or a power reduction input on a static memory. 662-1980w